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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,755	09/17/2003	Sterling Smith	MSS0007-US	3830

7590 03/01/2007

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,755	SMITH, STERLING	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12-04-06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7,9,10 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7,9,10 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *attached drawing*.

DETAILED ACTION

The amendment filed on 12-04-06 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Peterson et al. (US 5,926,217). See attachment.

Regarding claim 19, figure 3 of Peterson shows an electronic circuitry, comprising: a first capacitor (111) for capacitively coupling an analog image signal (Vdet) to a first node (N1); a resistor (119) electrically connected between said first node (N1) and a second node (N2); a second capacitor (121) electrically connected between said second node (N2) and a ground node; and a switching device (135) connected between said second node and a reference level (Vclamp); wherein said resistor and said second capacitor form a filter for processing said analog image signal and providing a processed image signal at said second node, and said switching device is controlled by a clamping signal, not shown, to clamp said second node at a clamping voltage (Vclamp) with reference to said reference level during a clamping interval. The switching device (135) that is equivalent to the switching device (M9) in figure 4 is a transistor having a drain connected to the internal node, a source connected to the reference voltage and a gate controlled by a clamping signal (Vclmp).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US 5,926,217) further in view of Kunugi et al. (US 4,980,914) and Obie (US 5,038,096).

Regarding claims 1, 3 and 4, figure 3 of Peterson shows an interface circuit of a display chip comprising an input node receiving an analog image signal with a display resolution; a resistor (117), a capacitor (121) and a switching device (135) connected between the internal node and a reference level (Vclamp). The resistor (117) and the capacitor (121) form a filter for processing the analog image signal and providing a processed image signal at said internal node, and said switching device is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval. Figure 3 of Peterson does not show that the resistor is variable. Figure 13 of Kunugi shows a low-pass filter comprising a variable resistor (3-14) and a capacitor (3-15) for changing the frequency characteristic of the signal i.e., for filtering high out frequency signal and varying the bandwidth of the signal. Therefore, it would have been obvious to one of ordinary skill in the art to replace the fixed low-pass filter of Peterson with the variable low-pass filter taught by Kunugi for being able to adjust the bandwidth of the image signal. The switching device (135) that is equivalent to the switching device (M9) in figure 4 is a transistor having a drain connected to the internal node, a source connected to the reference voltage and a gate controlled by a clamping signal (Vclmp).

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie (US 5,038,096) in view of Peterson et al. (US 5,926,217) and Kunugi et al. (US 4,980,914).

Regarding claims 15 and 16, figure 1 of Obie shows an interface circuit of a display chip comprising an input node receiving an analog image signal a low-pass filter (112) and an ADC unit connected to the internal node for converting the processed image signal to a digital image signal. However, the circuit of figure 1 of Obie does not show that the low-pass filter

(112) having a variable resistor, a capacitor forming a low-pass filter for providing a low-pass filter having adjustable bandwidth. Therefore. It would have been obvious to one of ordinary skill in the art to replace the low-pass filter (112) of Obie with the adjustable filter of the combination circuit taught by Peterson and Kunugi for being able to adjust the bandwidth of the circuit in response to the display resolution. Note that it is well known to one of ordinary skill in the art that the display resolution is related to the bandwidth of the filter. By adjusting the bandwidth, the resolution is adjusted (see US 20040071363 [0942]; 20030060712, abstract).

Claims 7, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US 5,926,217) in view of Kunugi et al. (US 4,980,914) and Kwon et al. (US 6,724,245).

Regarding claims 7, 9, 10, the combination of figure 3 of Peterson and figure 13 of Kunugi show an interface circuit of a display chip comprising an input node, an a first variable resistor a capacitor and a switching device except for the that there is a variable resistor coupled between the internal node and the ground node. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) control by signal (Vbias) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching device (transistor M9 or transistor 135) of Peterson with the clamping circuit comprising a variable resistor and a switching device taught by Kwon for adjusting the voltage at the internal node. The connections of these two components are clearly shown in figure 1 of Kwon. Note that the first variable resistor (3-14) and a capacitor (3-15) taught by Kunugi form a low-pass filter; the switching device (M9) in figure 4 of Peterson or switching device (N2) of Kwon is a transistor having a drain connected to the internal node, a source connected to the reference voltage and a gate controlled by a clamping signal.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie (US 5,038,096) in view of Peterson et al. (US 5,926,217), Kunugi et al. (US 4,980,914) and Kwon et al. (US 6,724,245).

Regarding claims 17 and 18, figure 1 of Obie shows an interface circuit of a display chip comprising an input node receiving an analog image signal a low-pass filter (112) and an ADC unit connected to the internal node for converting the processed image signal to a digital image signal. However, the circuit of figure 1 of Obie does not show that the low-pass filter (112) having a first variable resistor, a capacitor and forming a low-pass filter for providing a low-pass filter having adjustable bandwidth, a second variable resistor coupled to the internal node and the switching device for adjusting the voltage at the internal node. The combination of Peterson, Kunugi and Kwon includes all the above elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the low-pass filter (112) of Obie with the combination circuit of Peterson, Kunugi and Kwon for having a variable low-pass filter comprising a clamp circuit that can adjust the voltage at the internal node. Note that the variable low-pass filter of Peterson, Kunugi and Kwon provides adjustable bandwidth and it is well known to one of ordinary skill in the art that the display resolution is related to the bandwidth of the filter. By adjusting the bandwidth, the resolution is adjusted (see US 20040071363 [0942]; 20030060712, abstract).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US 5,926,217) in view and Kwon et al. (US 6,724,245).

Regarding claim 20, figure 3 of Peterson shows an interface circuit of a display chip comprising an input node receiving an analog image signal with a display resolution; a resistor (117), a capacitor (121) and a switching device (135) connected between the internal node and a reference level (Vclamp). The resistor (117) and the capacitor (121) form a filter for processing the analog image signal and providing a processed image signal at said internal node, and said switching device is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval. Figure 3 of Peterson does not show a variable resistor connected between the second node and the switch device. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) control by signal (Vbias) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the

voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching device (transistor M9 or transistor 135) of Peterson with the clamping circuit comprising a variable resistor and a switching device taught by Kwon for adjusting the voltage at the internal node. The connections of these two components are clearly shown in figure 1 of Kwon.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie (US 5,038,096) in view of Peterson et al. (US 5,926,217) and Kwon et al. (US 6,724,245).

Regarding claim 21, figure 1 of Obie shows an interface circuit of a display chip comprising an input node receiving an analog image signal a low-pass filter (112) and an ADC unit connected to the internal node for converting the processed image signal to a digital image signal. However, the circuit of figure 1 of Obie does not show that the low-pass filter (112) having a switching device for clamping the second node with a reference level. Figure 3 of Peterson shows an interface circuit of a display chip comprising a low-pass filter including a clamping circuit for resetting the voltage of the output node of the low-pass filter (Peterson, col. 5, lines 27-29). Therefore, it would have been obvious to one of ordinary skill in the art to replace the low-pass filter (112) of Obie with the low-pass filter taught by Peterson for being able to reset the output node of the low-pass filter as required.

Regarding claim 22, the combination of Obie and Peterson includes all the limitations of claim 22, except for the limitation that there is a variable resistor connected between the second node and the switching device. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) control by signal (Vbias) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching device (transistor M9 or transistor 135) of Peterson with the clamping circuit comprising a variable resistor and a switching device taught by Kwon for adjusting the voltage at the internal node. The connections of these two components are clearly shown in figure 1 of Kwon.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

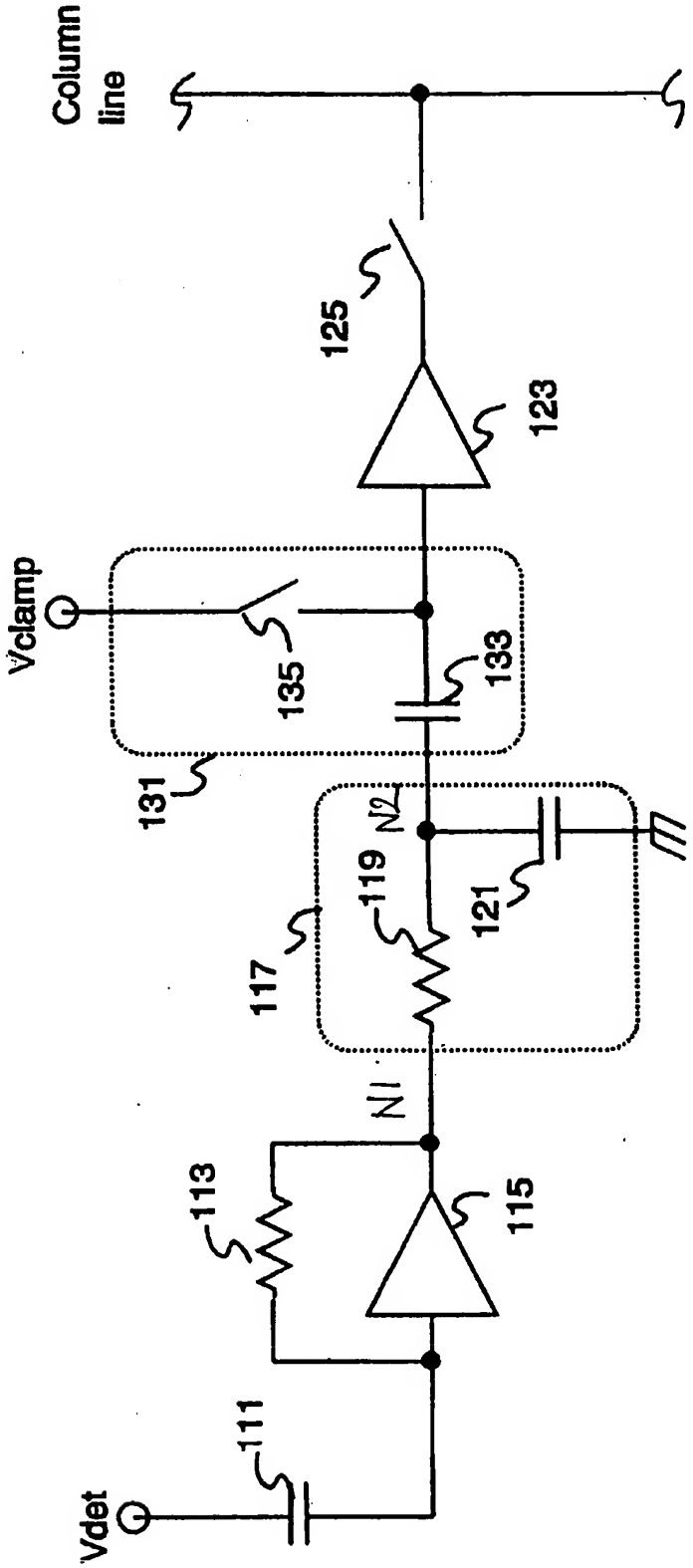
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen
02-21-07

TUAN T. LAM
PRIMARY EXAMINER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133
131
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119
121
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N1
113
115
111
Vdet

Fig 3